JarnisTech's Glass PCB Process Capability

Process Module	Item	Specification / Capability
Electrical Testing	Test Type	O/S, RC, LC
	Minimum Test Pitch	50 μm
	Minimum Test Pad Size	35 μm
	Dicing Die Size	1×1 mm × 0.4T
	Dicing Accuracy	＜10 μm
	Front Side Chipping	＜15 μm
	Back Side Chipping	＜20 μm
Plating	Through-Hole Aspect Ratio	1:05
	Plated Through-Hole Copper Thickness	≥10 μm
	Blind Via Aspect Ratio	1:01
	Dimple Depth	＜10 μm
	Surface Finish Type	ENEPIG, ENIG
	Metal Types	Cu, Ti
	Seed Layer Thickness	Cu: 3 μm; Ti: 100 nm
PVD (Metal Deposition)	Minimum Hole Diameter	50 μm
	PVD Aspect Ratio	1:05
	Deposited Metal Materials	Cu, Ti
	Step Coverage	3.00%
	Adhesion Strength	Cross-Cut: 5BPull Strength: ＞6 N/cm
	Sheet Resistance Tolerance	10%
	Film Uniformity	＞93%
TGV (Through Glass Via)	Hole Type	Through Hole
	Hole Pitch	100 μm
	Minimum Hole Diameter	30 μm
	Hole Circularity (@50 μm diameter)	95%
	Aspect Ratio	1:15
	Repeatability	±1 μm
	Positioning Accuracy	±3 μm
	Missing Hole Rate	2 ppm
Photolithography	Minimum Resolution	6/6 μm
	Line Width Tolerance	±10%
	Alignment Accuracy	5 μm
	Front-to-Back Registration Accuracy	7 μm
	Photoresist Thickness Uniformity	±10%
	Window Opening Size	30 μm
	Minimum Pitch	80 μm